

Unique Technology for Exponential Growth

Dr. Shay Wolfling, CTO September 2022

Dr. Shay Wolfling

Chief Technology Officer



Joined Nova as CTO in 2011.

R&D manager at KLA-Tencor-Belgium, leading multidisciplinary metrology & inspection projects.

Founder and VP R&D of Nano-Or-Technologies, a start-up company with a proprietary 3D optical technology, acquired in 2005.

PhD in physics from the Hebrew University.





NOKA INVESTOR

Technology Trends



Key Trends

Exponential growth in data generation

- Higher performance IoT Edge Computing with less power and space
- Compute needs for AI expanding decision intelligence, generative AI & constant optimization
 - Data Fabric breaking data silos

There is more than a single track forward

- Increasing Diversity of development tracks (Both leading & trailing)
- FinFET variants, Nanosheets, SOI, New materials, Analog, In-memory computation and more
 - Chiplets and Advanced Packaging

lova proprietary information

System integration (Device-Technology Co-Optimization)



Source: Ime



Traditional Scaling Gets a Boost



Technology Node (nm)

 Linear scaling is only part of the way forward

- More than Moore is essential:
 - New integrations
 - Novel materials
 - True 3D device and system



Solutions & Technology Inflections

	Inflections	Key value
Patterning	High NA EUV, Additive patterning	Density
Logic transistor	New architectures – Nanosheet, Forksheet, Complementary FET	Performance, Density, Power & Cost
Interconnect	Buried Power Rail, new materials , selective process	Performance, Power
3D NAND	Multi-Decks , Logic over / under memory, Increasing bits per cell	Performance, Density, Power & Cost
DRAM	EUV adoption, 3D DRAM	Performance, Density, Power & Cost
Packaging	Heterogenous integration , System level optimization	Performance, Density, Power & Cost

INVESTOR DAY 2022

NO





Chemical Metrology

Measure Chemical Solutions

Rather than on Wafer

Plating Bath Clean & Etch Composition

Electrochemical + Plating	
Wafer	
Plating Solution	
Metal Source	

Main components:

Acids, bases, organics

Secondary components:

Contaminants, breakdown products, leftovers



Key Challenges





Memory – 3D NAND Process Challenges

Dimensional

- 1. Full profile per deck and in total
- 2. Logic under Memory cell
- 3. Bottom parameters
- 4. Tiers and liner thickness
- 5. Tilt and Overlay between decks

Material

- 6. Dielectric composition & thickness control
- 7. Channel Poly Si crystallinity & grain size
- 8. Channel sidewall
- 9. Chemical residues
- 10. Stress management

Single Deck



> 400 Tiers

> 20um thickness

Logic under Memory

Triple Deck



From Single Deck to Multi Deck



Memory – 3D DRAM Process Challenges

Dimensional

- 1. High-Aspect Ratio capacitor holes & supporters
- 2. Bottom gate parameters
- 3. Tight contact holes
- 4. Lateral selective etches for thinner capacitors

Material

69

- 5. Dielectric composition & thickness control
- 6. Higher dielectric constants
- 7. Material residues

Nova proprietary information

2D DRAM 2D scaling is not enough

Move to 3D DRAM-Same path as NAND



Logic Architecture -Process Challenges

Dimensional

- 1. Multiple nanosheets shapes, spacing & thickness
- 2. Thin deposition surrounding nanosheets
- 3. Buried structures
- 4. Local topography variations

Material

- 5. Si / SiGe uniformity
- 6. SiGe residues
- 7. Stress & strain on multiple nanosheets
- 8. Doping control

Nova proprietary information

70

Clear Architecture Evolution – Increased Complexity



Interconnect -Process Challenges

Dimensional

- 1. HAR Cu nano-TSV profile control
- 2. Topography for Wafer-to-Wafer bonding
- 3. Voids & Delamination
- 4. Surface roughness

Material

- 5. Via Pitch and CD too narrow for plated copper
- 6. Cobalt etch Single damascene
- 7. Cu fill Buried Power Rails
- 8. Cu, Ru & Co interconnects plating

New Architecture Backside Power Delivery Network & Hybrid-Bonding with Nano-TSVs



© Nova proprietary information

Packaging Process Challenges

Dimensional

- The move from 2.5D to 3D -Topography & Profile
- High aspect ratio structures
- Buried structures
- Local topography variations

Material

- Optimal plating
- Highly saturated copper bath management
- By-Products metrology
- Contaminants and photoresist leach control
- Dielectric composition & thickness control

Fan Out 3D-IC True 3D architecture and tighter chemistry requirements

Enabling Chiplets

INVESTOR DAY 2022

NOVA

Metrology Challenges

Process Complexity



INVESTOR DAY **2022**

NO

Nova Solutions





Dimensional Metrology

Multi-Channel Integrated Metrology Combining Normal Incidence & Oblique Spectral Interferometry PRISM



Stand Alone performance in IM Extending Nova IM leadership An additional source of information to SR and SE

NOVA

Unique

Critical Dimensions





Materials Metrology

X-Ray: XPS and XRF

VERAFLEX

 In-Line composition & thickness
 In-Line

 Market leading technology
 High volume manufacturing

In-line Raman

ELIPSON

In-Line stress, strain and crystallinity Measuring material properties optically In-line SIMS METRION



In line full Composition profile Bringing SIMS from Lab to Fab

Material Properties



Chemical Metrology

ancolyzer Product Family



Automated separation technique whereby all components are separated before being measured Quantitative analysis using optics to directly measure component concentration

Chemical Analysis & Replenishment



77 © Nova proprietary information

Software Solutions



Across all Product Lines



Solutions for Nanosheets

Unique Technologies to Answer Key Challenges

Fin Patterning

- XPS Multiple nanosheets thickness
- SIMS Multiple nanosheets full profile
- OCD Multiple CDs along gate and fin HAR profile; Buried structures
- Raman SiGe stress post Etch of nanosheets

Gate Formation

- Raman SiGe deposition uniformity
- XPS LaO thickness
- SIMS Doping control



• XPS - High K thickness



METRION – Inline SIMS

Nanosheet Use Case: SiGe Deposition

The Challenge

Variations in nanosheet SiGe growth affect etch selectivity and impact device performance

METRION Solution

In-line SIMS monitors Ge concentration to ensure uniform deposition on each individual nanosheet and across the wafer





Solutions for Memory - 3D NAND Unique Technologies to Answer Key Challenges







VERAFLEX: XPS/XRF METRION: SIMS PRISM: OCD SI



Channel Hole Etch at Top Decks

ELIPSON:

Raman

- XPS ONON thickness & composition
- Raman- Channel poly crystallinity & Grain size
- OCD ONON & channel poly thickness



Pillar Sidewall Liner Deposition

- XPS Liner thickness
- SIMS Contamination detection & Individual layer thickness
- OCD Channel hole profile, bottom contact
- Nova FIT Machine Learning for 3D complexity

Zoom in- Solutions for 3D NAND



INVESTOR DAY **2022**

NOVX

Solutions for Packaging

Unique Technologies to Answer Key Challenges

Dimensions



- RDL CD and thickness
- Multi-Layer dielectric thickness
- TSV CD and depth
- Topography



Materials

- Al bond pad monitoring
- 3D Interconnect: TSV, hybrid bonding Cu2Cu
- High K composition & thickness
- Cobalt cap & liner monitoring

- Organic additive breakdown
- Additive by-product buildup
- Photoresist components leaching
- Bath cross-contamination
- Bath replenishment



ancolyzer chemical metrology Packaging Use Case: High Aspect Ratio Plating

Concentration 5 10 0 15 20 Measurement Suppressor Accelerator I eveler VESTO

Excellent Control, Accuracy and Reproducibility

DAY

The Challenge

Electroplated Copper micronsize vias plating quality is strongly affected by the changes in the plating solution

ancolyzer Solution

Automated inline analysis of inorganics, organic additives, breakdown-products and contaminants

Nova Future Directions





Summary



Multiple technology inflections

Logic- architecture evolution with increased complexity

3D NAND - multiple decks

DRAM - Going to 3D

Packaging- tighter process windows

Dimensional, Material and Chemical implications



Enhanced by physical modeling and machine learning

Holistic technology portfolio for all device segments

Solutions



Ongoing Innovation to Support Exponential Growth





NO ROCESS INSIGHT

0

Thank You