Scatterometry for Gate-All-Around (GAA) Technology Enablement

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ABSTRACT

The future of logic silicon extension lies at the heart of Gate-All-Around (GAA) developments (1). Due to the increasing limitations in further FinFET flow extension, research groups worldwide are fabricating vertical and horizontal nanowire (NW) integration schemes. The horizontal NW are of great interest due to their integration similarity to the existing FinFET integration flow (2). This in turn allows to extend the usage of existing process and metrology platforms and reduce the cost of shifting to a new technology. Though the integration changes seem to be limited, they spring numerous new obstacles for fab metrology. As new parameters of interest emerge, the metrology capability needs to achieve higher performance and develop new solution methods (3) (4).

This paper focuses on several key process steps that are different from the FinFET process flow and discusses the OCD (Optical Critical Dimension) scatterometry capabilities. At the nanowire release step, a SiGe dummy layer is removed by dry etching, leaving the active silicon nanowires. Detailed metrology of these nanowire profiles and thicknesses is required to make sure that the device can perform to the expected specifications. To examine the scatterometry performance of this application, a Design of Experiment (DoE) was created at multiple process steps.

At the fin formation process step, we describe a DoE condition of applying silicon - silicon germanium (Si-SiGe) multi-layer deposition splits where the SiGe layer thicknesses are changed between wafers. It is further shown how scatterometry can be used to sustain the X-Ray Reflectivity (XRR) accuracy and ensure higher sampling capability. A fin-reveal DoE was used to alter the total recess depth, allowing the lower SiGe layer to be revealed in varying amounts in the preparation for the later SiGe release etching step. We discuss a process condition where an Atomic Force Microscope (AFM) and scatterometry can both be used as well as demonstrate a condition where AFM has limited capabilities and one can only use scatterometry. The final process reported in this paper is the Nanowire Release (NW Release) etching method in which the SiGe is released while the silicon NW remains. The DoE consists of two etching methods, each providing a different NW profile. We explain how scatterometry can monitor the nanowire profile by using a specific target design. Finally, we discuss the improved accuracy that becomes possible owing to the Transmission Electron Microscopy (TEM) rich sampling.

Keywords: scatterometry, Gate-All-Around, GAA, Nanowire Release, XRR, AFM, TEM.

1. INTRODUCTION

Horizontal Gate-All-Around (GAA) is a natural evolution of the standard FinFET flow. It allows to obtain the benefits of GAA with minimal non-drastic modifications to the known FinFET process flow (Figure 1). The dominant improvement is in the electrostatic control that is achieved by the work function metal (WFM) wrapped around the nanowire (Figure 2). The electrostatic improvement enables addressing a more aggressive gate length (Lg). An additional benefit is obtained by the new capability of stacking more active volume per device. This means more nanowires stacked one on top of the other in the vertical direction, leading to a higher drive current and reducing the number of tracks per device. The effective cell area can be reduced by 16% while shifting from six-track to a five-track device (Figure 3).

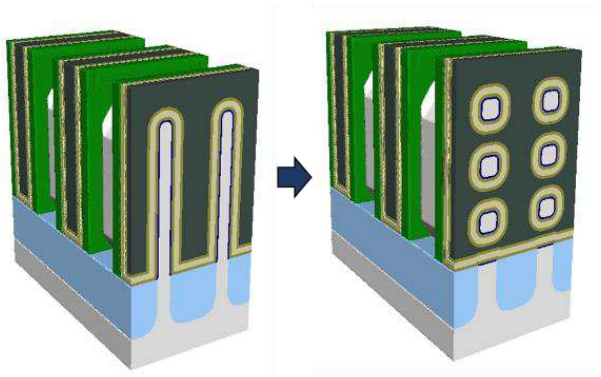

Figure 1. Natural shift from FinFET to a horizontal Gate-All-Around (GAA). Images courtesy of Coventor.

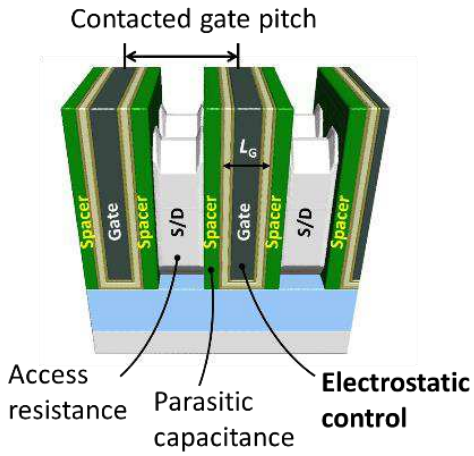

Figure 2. GAA improved electrostatic control enabling a more aggressive Lg scaling. Images courtesy of Coventor.

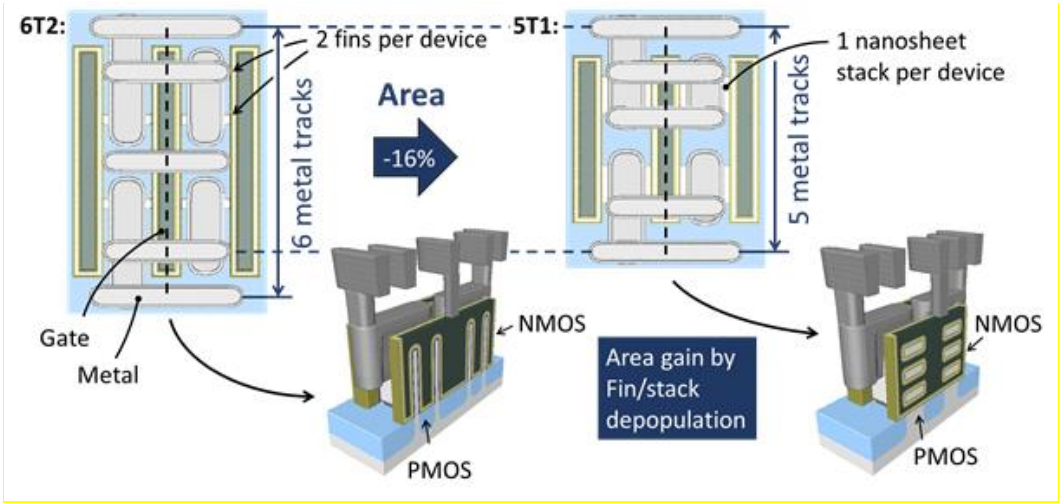

Figure 3. More active volume and higher drive current (with cell area reduction). Images courtesy of Coventor.

2. HORIZONTAL GAA PROCESS STEPS AND METROLOGY NEEDS

As mentioned earlier, the GAA process flow is quite similar to the FinFET flow. In this section, we describe the process steps that are unique to the GAA process flow and differentiate it from the standard FinFET flow.
The first distinction is the super lattice epitaxial growth of silicon germanium ($Si_{0.7}Ge_{0.3}$) and silicon layers (Figure 4a). In the flow presented, the two silicon germanium layers, 10nm thick each, were used as sacrificial layers. The epitaxy (Epi) silicon layers that served as active regions, have a 10nm thick bottom silicon layer and a 13nm thick top silicon layer. The Epi layers require tight thickness control; silicon thickness is one of the properties that control the device drive current. On the one hand, the SiGe thickness is tailored to provide the required gap between the nanowires; on the other hand, it is necessary to maintain the fins aspect ratio.

After a standard self-aligned double patterning, we obtain grating with a periodicity of 45nm. The process continues to the Fin Etch, STI fill, and Fin Reveal steps, producing fins that are 45nm in height and 20nm in line width (Figure 4b). Total recess depth is an important parameter to measure as it indicates whether the bottom SiGe layer has been exposed for the subsequent process step, in which the sacrificial SiGe layer is removed.

The following process steps are quite similar to the standard flow and include dummy gate patterning, spacer formation, fin recess, embedded source drain epitaxy (SD Epi), ILD0 fill, ILD0 CMP, and dummy gate removal. We have reached the process step where the silicon/silicon germanium fins are exposed within the gate trench. As we proceed with the lateral silicon germanium etch, only two floating silicon nanowires remain within the trench. This step is known as Nanowire Release (Figure 4c): the silicon nanowires are now suspended by the Gate Spacer between the two sides of the trench. The DOE process flow ends at the HK/IL (HfO2/SiO2) gate dielectric deposition step.

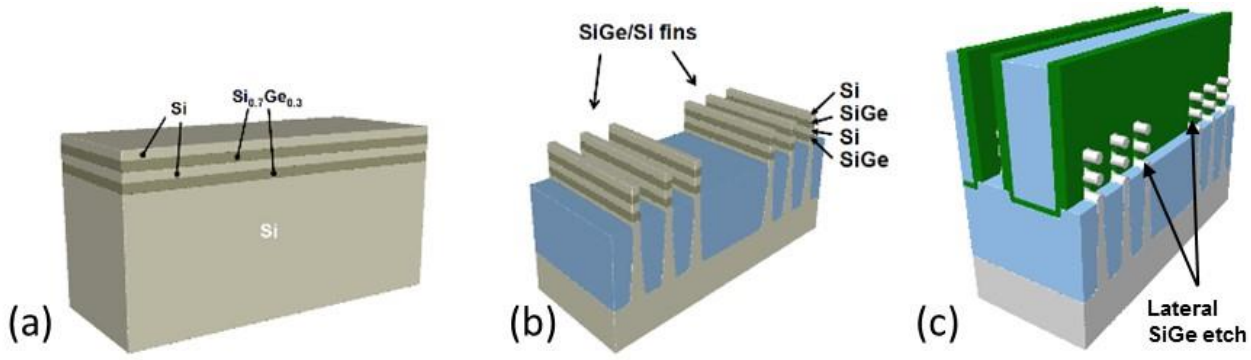

Figure 4. (a) SiGe/Si epitaxy, (b) Fin Reveal, (c) Nanowire Release. Images courtesy of Coventor.

3. GAA SUPER LATTICE GROWTH: THIN FILM METROLOGY

In the design presented, the GAA supper lattice consists of four SiGe and Si layers. The complete stack needs to be measured once the epitaxy growth ends, to insure that Epi growth has provided the planned thicknesses. Out of 15 wafers that were used in the DoE, 14 were in a POR process condition (10nm) and one had a split condition for the epitaxy of two SiGe layers, providing a shift of -4nm from the POR. All 15 wafers were measured using an X-Ray Reflectometer (XRR) as reference metrology. The XRR measured three radial distances on each wafer: 0, 50mm, 100mm. The system tested was a multichannel scatterometry system (an OCD). The OCD used a full wafer map measurement sampling technique. Both the XRR and OCD provided results for each Epi layer. Comparing the OCD and XRR results, we obtained an excellent match between the systems for each Epi layer (Figure 5). A SiGe condition with an equivalent resolution in both systems, was detected (<0.5nm for both SiGe layers).

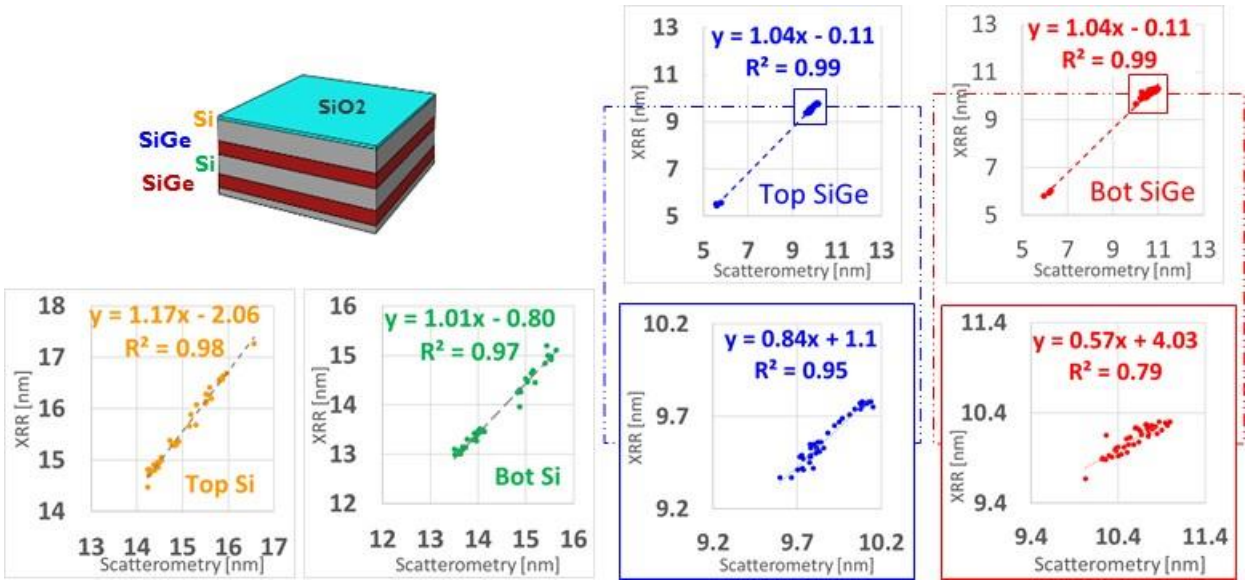

Figure 5. OCD vs XRR matching (the SiGe split condition is detected). Good matching between the systems also for the Si Epi layers with a <3nm range. Data points consist of 15 wafers in the center , mid-range (50mm), and wafer edge (100mm), which corresponds to a total of 45 data points.

Once the OCD performance is proven, we can benefit from the high sampling capability of the OCD system. The full wafer map results show that a SiGe split condition has minimal effect on the thickness range of each wafer and that both slots show a smooth cross-wafer distribution pattern (Figure 6).

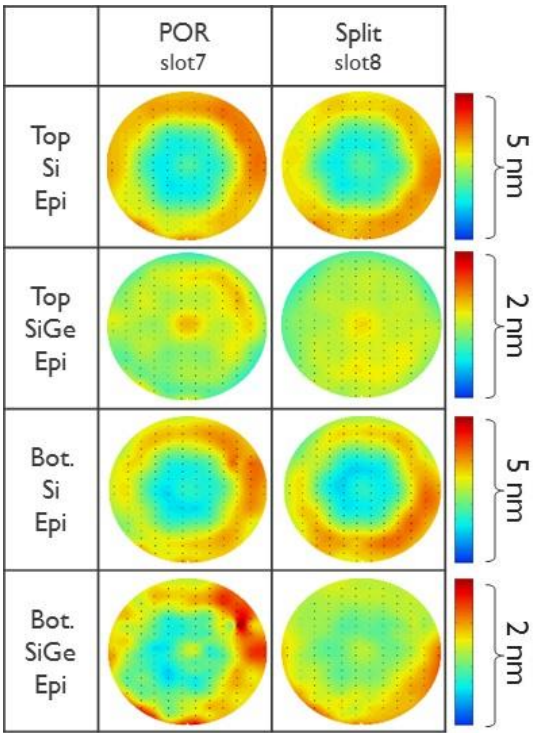

Figure 6. The OCD full wafer sampling capability allows to compare the parameter distribution patterns within wafer (WiW) and wafer-to-wafer (W2W), proving independence from the SiGe split condition.

4. GAA FIN REVEAL METROLOGY

In the standard FinFET flow, Fin Height is determined by the amount of the STI SiO2 recess. This is different from the GAA Fin Reveal process step where the purpose of the STI SiO2 recess is to expose the bottom sacrificial SiGe layer. The bottom SiGe layer must be exposed completely during this etch (to be removed at a later step) thus physically separating the lower silicon nanowire from substrate. This explains the importance of controlling the GAA Fin Reveal with high accuracy for any given Fin line and space. This property can be accessed by several metrology techniques, such as TEM, AFM, and OCD. TEM is a destructive technique and is considered here only as reference; it is not used for high-volume manufacturing. AFM is a direct, non-destructive technique that does not require modeling. The limitations of AFM is tip size when considering narrow trenches and small periodic structures, as in our Process of Record (POR) target.

To examine the benefits of using OCD for calculating the Recess Total Depth, a design of experiment was constructed where both the STI SiO2 fill and SiO2 etch were split to provide four different total recess depths. OCD was able to detect the split condition and identify which condition was appropriate to expose the bottom SiGe layer completely (Figure 7).

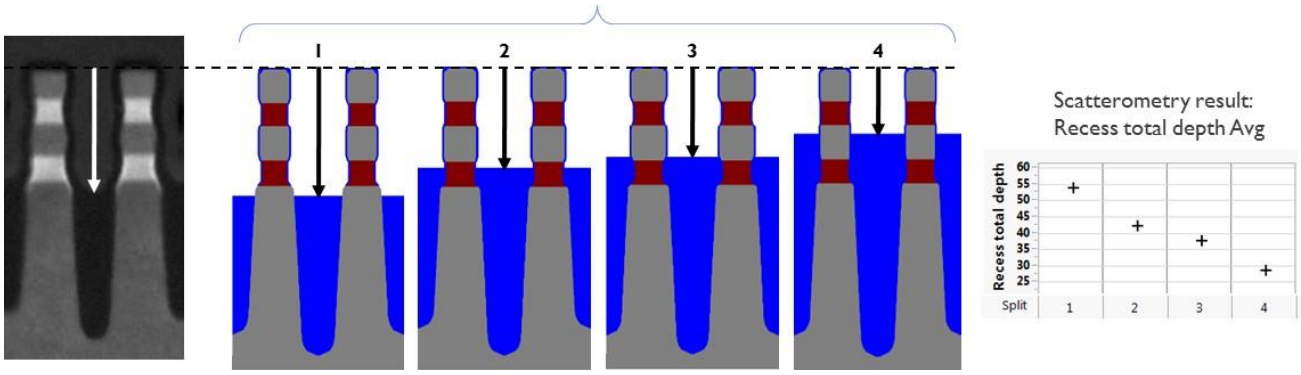

Figure 7. OCD tracks the GAA Fin Reveal split condition. Image on the left shows the representative TEM profile. The results demonstrate that process split #1 is properly tuned and that the bottom SiGe layer was fully exposed. The narrow space and high aspect ratio of the Fin at split#1 do not allow the AFM measurement to be taken due to the tip dimension.

To validate the OCD results, we collected both AFM and OCD results from central dies of 13 wafers. The recess total depth varied within the range of conditions 1, 2 and 3. Based on the AFM 3 sigma trench variability, conditions 2 and 3 are within the AFM measurement capability (Figure 8). There is a good agreement between the AFM and OCD results; a small discrepancy can be explained by the limited number of trenches measured by AFM compared to several hundreds of trenches within the collection spot that were measured by OCD.

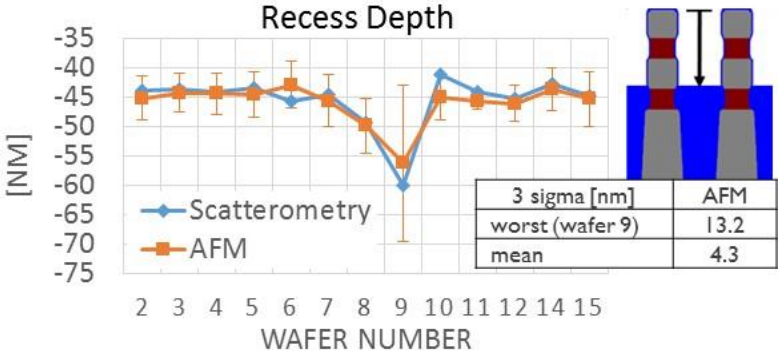

Figure 8. OCD shows a good agreement with the AFM results at the wafer center. AFM measured a limited sampling of only 6 trenches. The AFM 3 sigma error bar indicates the trench variability. The OCD averages a few hundred trenches within the collection spot and therefore does not have a corresponding error bar. The OCD precision is well below 1nm for the recess depth parameter.

5. GAA NW RELEASE METROLOGY

NW Release is the last process step where the active channel width and height are defined. These properties are important factors for determining the drive current, thus making metrology for this process step a key enabler for GAA fabrication. In this experiment we decided to provide a metrology solution at post-HK/IL deposition (Figure 9a). The HK/IL thin film (3nm) does not alter the metrology capability but it does provide a clean NW warped with a thin passivation layer. This in turn prevents any further NW oxidation during the experiment. The HK layer also allows a simple examination of the TEM cross-sections, including one at low resolution, by easily detecting the HK darker view that warps all the stack exterior boundaries (Figure 9b).

In this study our attention was focused on four key parameters: the top and bottom NW width (CD) and height; the top gap between two nanowires, and the bottom gap between the bottom nanowire and the substrate (STI silicon line) (Figure 10).

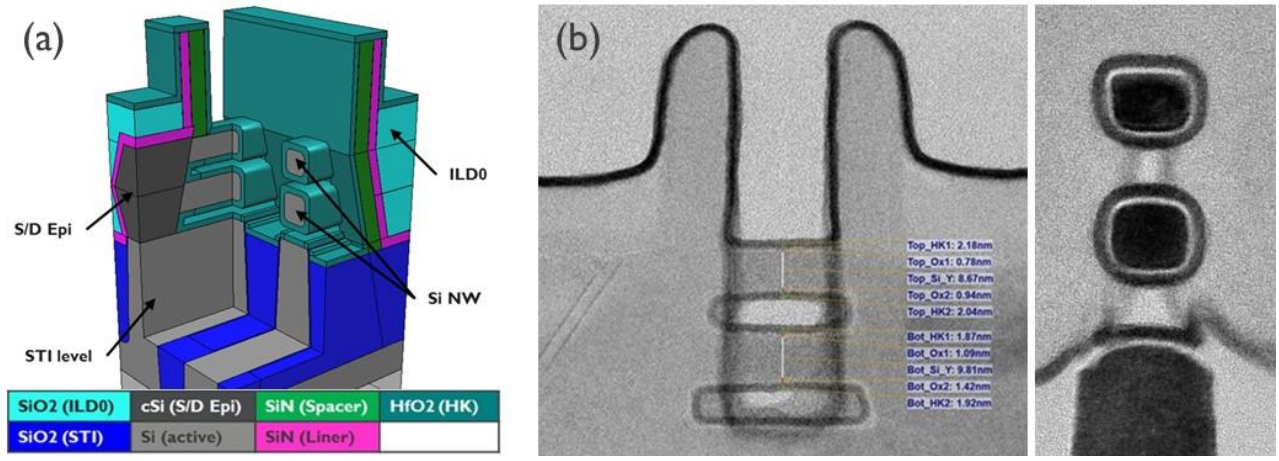

Figure 9. (a) NW Release stack and material description at post-HK/IL deposition. (b) TEM images showing the high contrast of the dark HK layer warping all exterior stack surface (ILD0 and Gate Spacer) and surface around the cross-section of the two nanowires (on the right image).

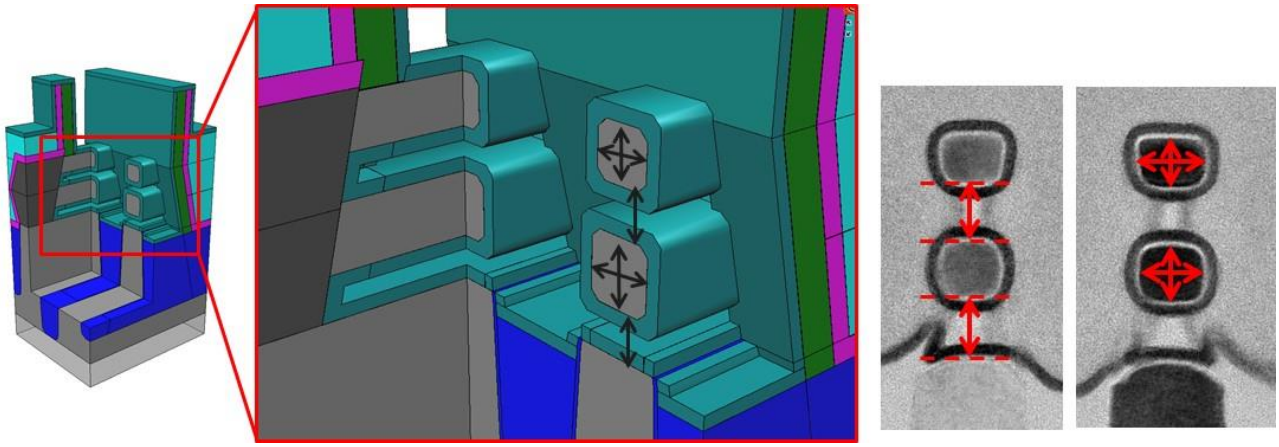

Figure 10. NW Release key parameters are marked with black arrows in stack model description, and presented as arrows, on the TEM cross section images on the right.

6. GAA NW RELEASE TARGET DESIGN

To examine the NW Release metrology potential in providing all key parameters with a sufficient accuracy, we suggest examining the target design. In previous SPIE, we presented an example of the OCD target design contributing to key parameter metrology in the SAQP pitch walking case (5). The following toy model provides a simplified illustration of the motivation behind the idea. The model is created using two simple shapes: a silicon box representing nanowire (or fin) and a SiGe box representing the SD Epi. The four different toy model configurations are presented in Figure 11a. If we plot the sensitivity, correlation, and accuracy theoretical analyses of the model, one can observe – as is also intuitively clear – that as we reduce the SiGe box, the metrology performance of the Silicon box parameter improves (Figure 11b).

This observation concept has been applied to the NW Release application where our goal was to maximize the nanowire target parameters. To simplify the DoE, a mask-based target design that creates or eliminates the SD Epi regions, was omitted for some of the wafers by skipping certain process steps. The process steps that were fully or partially skipped are Fin Recess and SD Epi growth, as shown in the table below (Figure 12). By this DoE we effectively obtained three distinctive target designs (i.e., different models or applications). Model A represents the case where Fin is not etched and no SD Epi is grown. Consequently, model A has the longest silicon nanowires and is expected to have the best sensitivity to the target parameters. Model C represents the POR condition; it has the SD Epi grown, which replaces the Fins in the out-of-gate trench region. Model C has both a short Si nanowire and a large additional SD Si Epi that are expected to correlate or at least screen the NW sensitivity thus reducing target parameter metrology.

An important aspect of the model comparison test is its ability to assess each model's metrology accuracy and ensure that the test is performed in a similar condition: i.e., all models being defined as accurately as possible, use similar inputs and have equivalent fitting levels. To satisfy these requirements, a large TEM sampling is needed for both defining these complex geometries and testing each model or wafer results. For that purpose, an automated workflow was used to create the TEM samples, images, and measurements. A large TEM sampling provides an added benefit of allowing to refine the OCD model. The TEM input can reveal unknown process effects that were not expected during preliminary process assessment. This is specifically true when dealing with multiple targets that were designed in an R&D facility. One such example is described in the case presented by Model A where a remaining SiGe/Si Fin was identified outside the gate area (Figure 13).

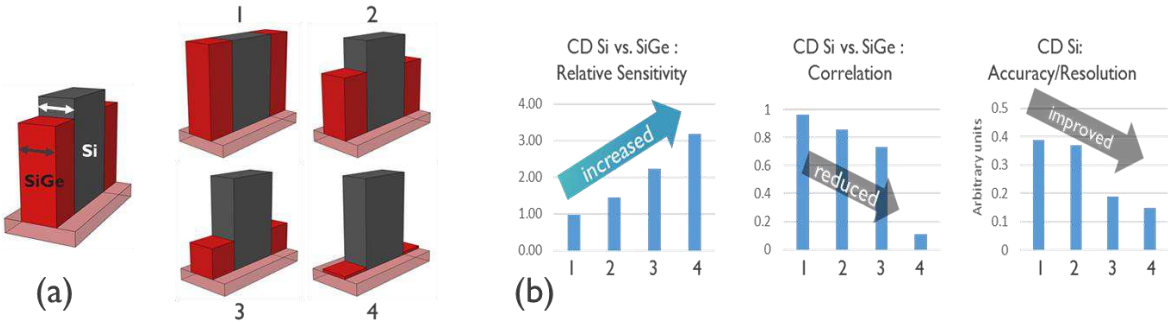

Figure 11. (a) The toy model and its four configurations. (b) Toy model theoretical analysis, showing improvement of Silicon metrology performance as the SiGe box size decreases relatively to the Silicon box.

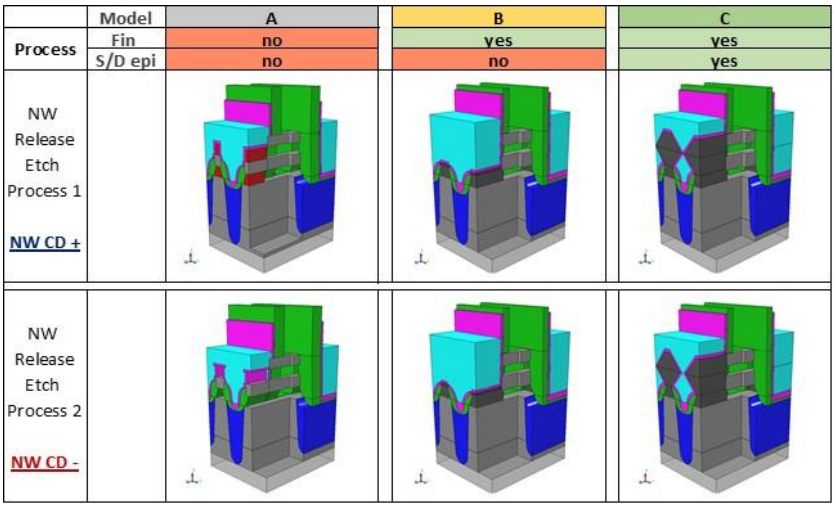

Figure 12. DoE for GAA NW Release, assessing the favorable design that should maximize the metrology performance of the NW target parameter. The two NW Release etch conditions provide a NW CD split, allowing comparison of the OCD results to a given reference (TEM).

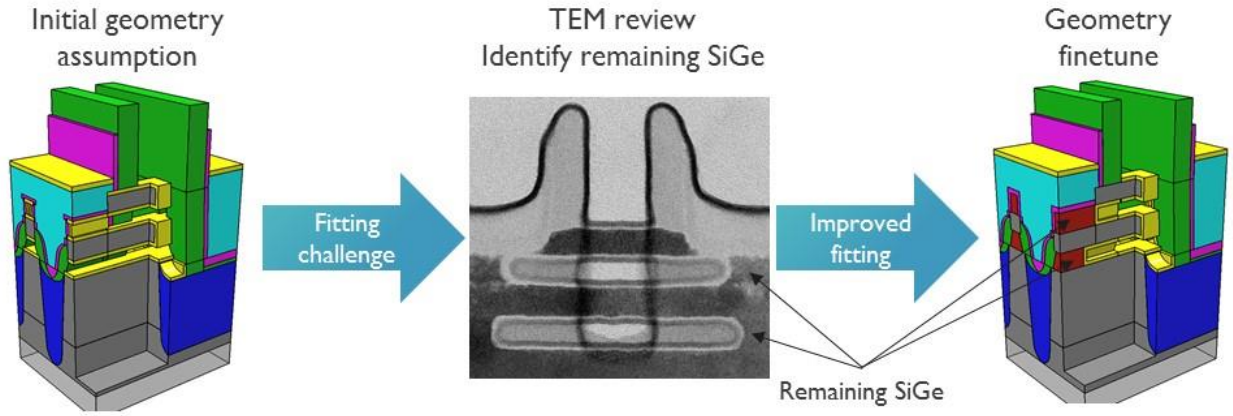

Figure 13. High TEM sampling helps refining the OCD model geometry and reveals whether a process deviation expected for the target design, had consistent effect across multiple dies.

7. GAA NW RELEASE RESULTS

This section discusses the results of OCD vs. TEM for models A and C. We have compared the nanowire average CD and average thickness for models A and C. For Model C wafers, for the top and bottom gaps, we had a split condition that originated at the super lattice growth process step.

Figures 14 and 15 demonstrate the representative models, TEM cross-sections, and the OCD vs TEM comparison charts. As can be observed in the Overlay charts of Model A, we obtained similar within-wafer (WiW) trends and wafer-to-wafer (W2W) split detection on both OCD and TEM (Figure 14). There is a limited TEM reference for Model C; however, a W2W CD split has been detected on both OCD and TEM. Model C is going to be further analyzed with an additional TEM, hence we are currently unable to compare the target design of models A and C to determine the more favorable one.

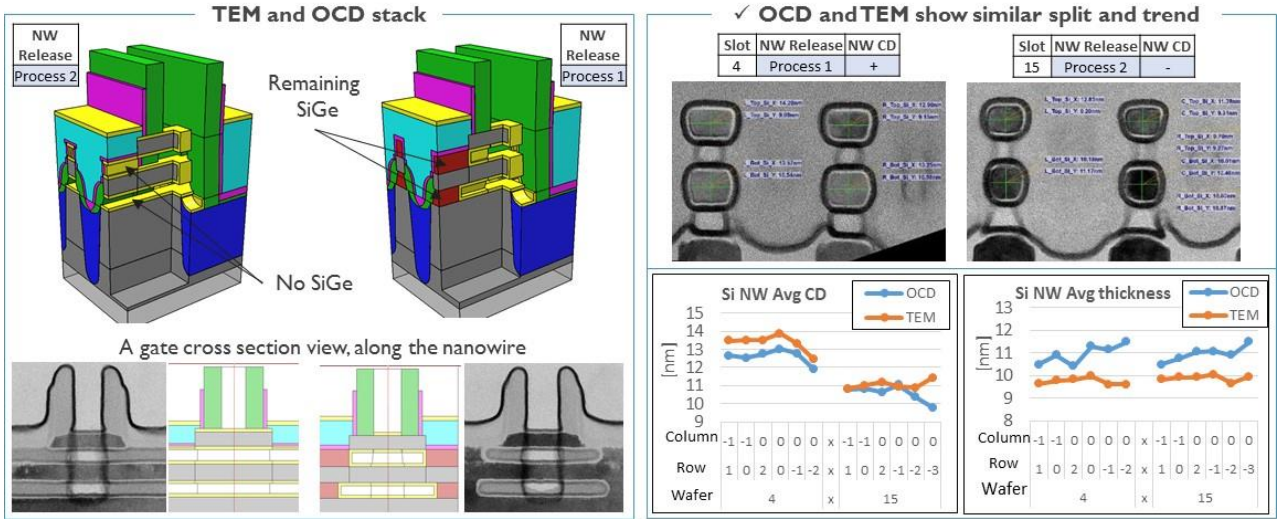

Figure 14. Model A. Left box represents the OCD model and the TEM gate cross section. Right box shows the target parameter as seen in the TEM image and the corresponding OCD vs. TEM overlay charts for the NW average CD and average thickness. The charts demonstrate similar WiW trend between OCD and TEM and both detect the W2W CD split.

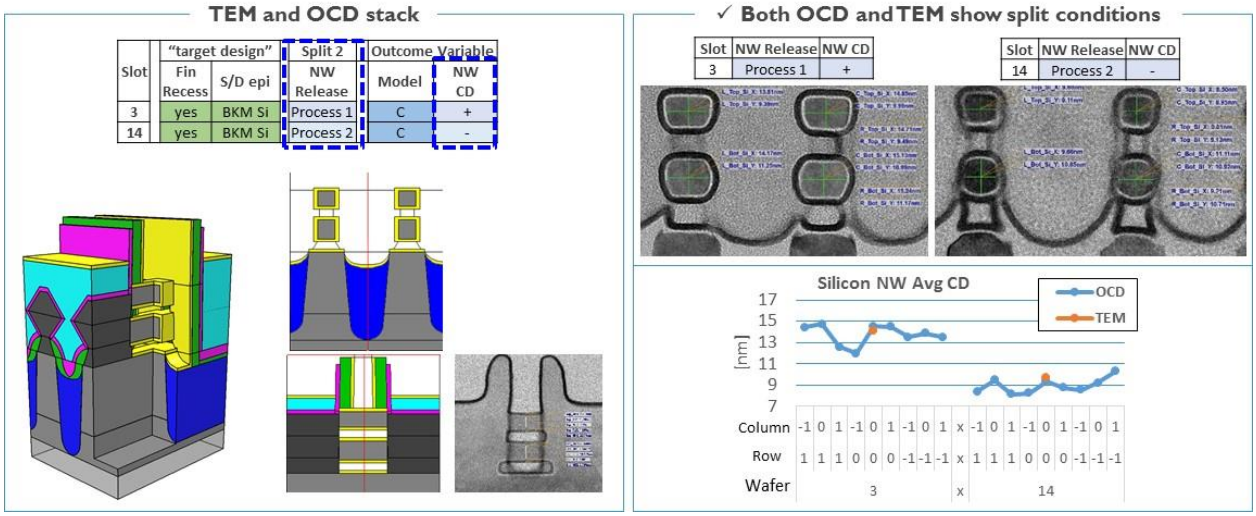

Figure 15. Model C. Left box illustrates the OCD model and the representative TEM at gate and fin cross-sections. Right box shows the target parameter as measured using a TEM and the corresponding OCD vs TEM (single point) overlay chart for the average NW CD. The chart demonstrates that both techniques identified the expected CD split.

8. CONCLUSIONS

GAA is a promising Silicon extension to the existing FinFET technology. We have illustrated how scatterometry can enable and boost the existing metrology capabilities at each unique metrology step of the new technology. It has been shown that OCD can provide the required analysis of each Epi layer of a superlattice stack, with an excellent matching to XRR. Both AFM and OCD have demonstrated the expected DoE tracking at the Fin Reveal step for the Etch Total Depth, with OCD providing the added capability of measuring narrow trenches with the same performance accuracy as shallow ones. We have introduced the concept of improving the NW release metrology for key parameters by using target design.

In one of the target design stacks it has been illustrated how well the OCD and TEM correspond on the detection of wafer splits and WiW trends. We plan to expand the study of target design and use an additional TEM reference so as to identify the preferred design that has improved metrology capability for the nanowire profile.

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